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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,555	07/17/2003	Bryan D. Boatright	2207/1012902	9247

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,555	BOATRIGHT ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed July 26, 2005 in response to PTO Office Action dated March 3, 2005. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 31-42 have been presented for examination in this application. In response to the last Office Action, claims 41 and 42 have been added.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 31-40 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-17 and 20 of U.S. Patent No. 6,678,807. Although the conflicting claims are not identical, they are not patentably

distinct from each other because all claim limitations of the application were previously recited by the aforementioned patent. As an example, the correspondence between application claim 31 and patent claim 15 is shown.

Application No. 10/620,555	Patent No. 6,678,807
31. A multiple store buffer forwarding apparatus, comprising: a processor having a write combining buffer, and	15. A system for multiple store buffer forwarding, comprising: a processor having a write combining buffer,
	the write combining buffer including: a comparator to receive and compare an incoming load operation target address with all cacheline addresses of existing write combining buffer entries, an address and data buffer coupled to the comparator, a data valid bits buffer coupled to the address and data buffer, a multiplexor coupled to the data valid bits buffer, and a comparison circuit coupled to the multiplexor;
a non-volatile memory coupled to the processor, said non-volatile memory storing instructions which when executed by the processor cause the processor to:	a non-volatile memory coupled to the processor to store instructions to be executed by the processor to:

execute a plurality of store instructions referencing a first memory region;	execute a plurality of store instructions;
execute a load instruction referencing a second memory region;	execute a load instruction;
determine that the second memory region matches a cacheline address;	determine that a memory region addressed by the load instruction matches a memory region corresponding to a cacheline address in a memory;
determine that the first memory region completely covers the second memory region; and	determine that a memory region data stored by the plurality of store instructions completely corresponds to the memory location in the memory specified by the load instruction; and
transmit a store forward is OK signal.	transmit a store forward is OK signal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 36 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Witt (US# 6,141,747)

Regarding claim 36, Witt teaches a load forwarding system similar to the claimed invention. The processor may include a load/store unit including a store queue memory (60) (col. 3, lines 2-13) to perform the load forwarding operations. A load/store unit searches a store queue for each byte accessed by the load, where the store queue is able to contain multiple store instructions. Load data may be forwarded from the store queue if the load data is stored therein, which relates to the determining step as claimed [col. 2, lines 12-14; here the matching of first and second memory regions is contemplated, and the covering of the second by the first is realized and produces the forwarding of data as claimed] . Forwarding may occur from up to N stores (where N is the number of bytes accessed by the load), meaning that the single load corresponds to up to maximum of N store instructions (col. 2, lines 2-22). Although the "transmit a signal indicating that store buffer forwarding is authorized" is not explicitly stated, Witt teaches that the data may be forwarded in order to increase the overall performance of the processor, and one of ordinary skill in the art would recognized that a signal to begin

the forwarding, as can be interpreted of the claimed recitation, would be inherent and necessary in order to carry out the operation of forwarding data.

Regarding claim 40, Witt teaches that although processor (10) is implemented into the computer system, processor (10a) can be implemented without affecting the computer system. Also, processor (10a) could be identical to processor (10), and thus contain their own individual resources such as cache memories, buses, etc. (col. 20, lines 58-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (US# 6,141,747) and Tanenbaum. The rejections are done in view of the Examiner's best interpretation of the claimed material.

Regarding claim 31, Witt teaches a load forwarding system similar to the claimed invention. The processor may include a load/store unit including a store queue (col. 3, lines 2-6). A load/store unit searches a store queue for each byte accessed by the load, where the store queue is able to contain multiple store instructions. Load data may be forwarded from the store queue if the load data is stored therein, which relates to the

determining step as claimed [col. 2, lines 12-14; here the matching of first and second memory regions is contemplated, and the covering of the second by the first is realized and produces the forwarding of data as claimed] . Forwarding may occur from up to N stores (where N is the number of bytes accessed by the load), meaning that the single load corresponds to up to maximum of N store instructions (col. 2, lines 2-22). Although the "transmitting a store forward is OK signal" is not explicitly stated, Witt teaches that the data may be forwarded in order to increase the overall performance of the processor, and one of ordinary skill in the art would recognized that a signal to begin the forwarding, as can be interpreted of the claimed recitation, would be inherent and necessary in order to carry out the operation of forwarding data.

The difference between the claimed subject matter and that of Witt, disclosed supra, is that the claim recites a non-volatile memory coupled to the processor, where the memory stores instructions for enabling store-forwarding operations. The system of Witt teaches the store-forwarding system, but fails to recite a memory that stores the instructions for performing such store-forwarding operations. One of ordinary skill in the art would recognize that the hardware load/store unit, in conjunction with the processor, is responsible for the store-forwarding system of Witt. Tanenbaum teaches that hardware and software are logically equivalent, in that whatever can be produced in hardware can be reproduced in software (page 11). One of ordinary skill in the art would also recognize that for a software program (instruction) to be repeated, a non-volatile medium such as a disk would be required to store the program. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Witt

and Tanenbaum before him at the time the invention was made to modify the hardware store-forwarding system of Witt to facilitate the software-based system of Tanenbaum, because then should small adjustments to the processing instructions be required, only the instructions (programs) themselves need to be altered and not the logical hardware, thus reducing operational costs.

Regarding claim 35, Witt teaches that although processor (10) is implemented into the computer system, processor (10a) can be implemented without affecting the computer system. Also, processor (10a) could be identical to processor (10), and thus contain their own individual resources such as cache memories, buses, etc. (col. 20, lines 58-67).

Response to Arguments

Applicant's arguments filed July 26, 2005 have been fully considered but they are not persuasive.

Applicant has argued on page 6 of the response that the Witt reference does not teach a "write combining buffer" in accordance with Applicant's needs for a write combining buffer, noted as:

> These two steps ensure that store buffer forwarding will be authorized only when the relevant data will be transmitted to memory in a single atomic transaction thereby ensuring data consistency in a multiprocessor environment. Witt overlooks the critical need to guarantee an atomic update of system memory in a multiprocessor architecture and Witt therefore fails to determine whether these two criteria are satisfied before permitting store-forwarding to occur.

Witt teaches a store queue that performs the operations as claimed, as noted above in the rejection, but has not been indicated to teach 'atomic update' as seen in the previous paragraph due to the phrase's absence from the claimed subject matter.

Applicant further argues on page 6 through paragraph 1 of page 7 that the Witt reference does not teach the determining steps as claimed, but merely "...describes forwarding the load data *if it is available*". The Examiner would like to point out that in regards to the determining steps of the claimed subject matter of claims 36 and 40, Witt teaches the determining steps in that the data is forwarded if the data is available based on the matching of memory regions, matching being that the first region 'covers' the second region. Data is only forwarded if the data is available due to the 'determining' by Witt that the regions overlap. The Applicant further argues that:

> when Witt performs store-forwarding, no steps are taken to ensure that all of the relevant store operations will become globally observed (GO) at the same time. Thus, in contrast to the present invention, Witt will not operate properly in a multi-processor architecture. Even though Witt states that his invention could be implemented in a multiprocessor environment (as the Examiner points out), Witt makes no provision to ensure that the results of a store-forwarded load operation, as executed by one of several processors, will yield predictable results when the forwarded data is supplied by a plurality of pending store operations.

Witt teaches multiprocessor environment as claimed, as noted above in the rejection as well as by Applicant's admission, but has not been indicated to teach 'globally observed' limitations as seen in the previous paragraph due to the phrase's absence from the claimed subject matter.

Applicant further argues that the Witt reference would not be proper because:

> The present application provides examples illustrating the erroneous behavior of store-forwarding operations in architectures similar to that of Witt. Summarizing those examples, if a given load operation is satisfied by store-forwarding from two different store operations, unpredictable results may occur in a multiprocessor environment if those two store operations are globally observed at different times.

Once again, Witt but has not been indicated to teach 'globally observed' limitations as seen in the previous paragraph due to the phrase's absence from the claimed subject matter.

Regarding Applicant's arguments regarding the rejection of claims 31 and 35, the Examiner has noted above that the Witt reference teaches the store-forwarding determination steps as claimed. Neither Witt nor Tanenbaum, has not been used to teach a 'single atomic transaction' as noted by the Applicant due to the phrase's absence from the claimed subject matter.

Allowable Subject Matter

Claims 41 and 42 are allowed over the prior art of record

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
October 13, 2005